PTO/SB/05 (08-03)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	*100-14310 (P04927-C1)*
First Inventor	*Terry Lines*
Title	*Depletion-Mode Transistor That Eliminates The Need To Separately Set The Threshold Voltage Of The Depletion-Mode Transistor*
Express Mail Label No.	EV342470547US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

031088 U.S. PTO 10/692255 102203

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification *Total Pages* 21
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross Reference to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to sequence listing, a table, or a computer program listing appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

4. ☒ Drawing(s) *(35 U.S.C. 113) Total Sheets* 20 (formal)
5. Oath or Declaration *Total Sheets* 2
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☒ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document *(if applicable)*
12. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Request and Certification under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☒ Other: Copy of Power and Change of Address 37 CFR 1.63(d)(4) and Letter to Examiner

18. *If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/824,653

Prior application information: *Examiner* Eugene Lee *Group Art Unit:* 2815

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☒ *Customer Number or Bar Code Label* **33402** or ☐ *Correspondence address below*

Name	Mark C. Pickering				
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Name(Print/Type)	Mark C. Pickering	*Registration No. (Attorney/Agent)*		36,239	
Signature			*Date*	October 22, 2003	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Box Patent Application, Washington, DC 20231.

FEE TRANSMITTAL

For FY 2004

Patent Fees are subject to annual revision.

EV342470547US

TOTAL AMOUNT OF PAYMENT	$770

Complete if Known	
Application Number	New
Filing Date	Herewith
First Named Inventor	Terry Lines
Examiner Name	Unknown
Group Art Unit	Unknown
Attorney Document No.	100-14310 (P04927-C1)

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge any fees or credit any overpayment under 37 CFR 1.16 and 1.17 which may be required by this paper to Deposit Account No. **502305**
LAW OFFICES OF MARK C. PICKERING

☐ Applicant claims small entity status. See 37 CFR 1.27.

2. ☒ **Payment Enclosed:**
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. -BASIC FILING FEE

LARGE ENTITY Fee Code	LARGE ENTITY Fee ($)	SMALL ENTITY Fee Code	SMALL ENTITY Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility	770
1002	340	2002	170	Design	
1003	530	2003	265	Plant	
1004	770	2004	385	Reissue	
1005	160	2005	80	Provisional	
				SUBTOTAL (1)	770

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims	Fee from below	Fee Paid
Total Claims	8 - 20 **	= 0	x 18	= $ 0
Independent	1- 3	= 0	x 86	= $ 0
Multiple Dep.			*	= $ 0

*** or number previously paid, if greater; for Reissues, see below:*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claim in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue ind. claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)	$0

FEE CALCULATION (continued)

3. Additional Fees

Large Entity Fee Code	Large Entity Fee	Small Entity Fee Code	Small Entity Fee		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for ex parte reexamination	
1804	920	1804	920	Requesting publication of SIR prior to Examiner action	
1805	1840	1805	1840	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1480	2254	740	Extension for reply within fourth month	
1255	2010	2255	1005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive-unavoidable	
1453	1330	2453	665	Petition to revive-unintentional	
1501	1330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention be examined (37 CFR 1.129(b)	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** $0

SUBMITTED BY

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Date: 10-22-03

By: Mark C. Pickering

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Express Mail Number EV342470547US

PTO/SB/35 (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Terry Lines
Title	Depletion-Mode Transistor That Eliminates The Need To Separately Set The Threshold Voltage of The Depletion-Mode Transistor
Atty Docket Number	100-14310 (P04927-C1)

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

10-22-03
Date

Signature

Mark C. Pickering
Reg. No. 36,239
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Terry Lines Appln. No.: Continuation of 09/824,653 Filed: Herewith For: DEPLETION-MODE TRANSISTOR THAT ELIMINATES THE NEED TO SEPARATELY SET THE THRESHOLD VOLTAGE OF THE DEPLETION-MODE TRANSISTOR	Group Art Unit: 2815 Examiner: E. Lee LETTER TO THE EXAMINER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a continuation of Application Serial Number 09/824,653 that was filed on April 3, 2003. The present continuation application presents claims 1-8 which are identical to claims 8-13 and 19-20, respectively, which were cancelled in the parent application.

In the parent application, the Examiner rejected claims 8-11, 19, and 20 under 35 U.S.C. §102(b) as being anticipated by Ariizumi et al. (U.S. Patent No. 4,578,694). In previously rejecting the claims, the Examiner pointed to transistor 11 shown in FIG. 4 of Ariizumi as constituting the first transistor of claim 1 (previous claim 8), and transistor 12 shown in FIG. 4 of Ariizumi as constituting the second transistor of claim 1 (previous claim 8).

In an amendment in the parent application, applicant noted that applicant was unable to find any discussion within Ariizumi that teaches or suggests that the

thickness of the gate oxide layer of transistor 11 is substantially less than the thickness of the gate oxide layer of transistor 12 as required by the claims.

In the Advisory Action mailed on August 20, 2003, the Examiner stated that if transistors 11, 12, and 13 were all the same type of transistor, it could be said that the gate oxides have the same thickness. Applicant previously noted, however, that at one point in the fabrication process, transistors 11, 12, and 13 appear to all be the same type of transistor.

The Ariizumi specification teaches:

> "[g]ate insulation layers (19), (20) and (21) and gate electrodes (22), (23) and (24) are respectively formed on channel regions of MOSFETs (12), (11) and (13). . . . Arsenic ion is implanted in the channel regions of MOSFET (11) and (13) in order to change the threshold voltage in the negative direction and changes MOSFETs (11) and (13) to D type MOSFETs." (See column 4, lines 19-29 of Ariizumi.)

Applicant notes that to be changed to a D (depletion) type transistor, the transistor must have previously been an E (enhancement) type transistor. Transistor 12 is an enhancement type transistor. As a result, at one point during the fabrication process, MOSFETs 11, 12, and 13 were all E-type transistors. Since transistors 11, 12, and 13 were all the same type of transistor at one point, it can be said that the gate oxides have the same thicknesses as noted by the Examiner.

In the Advisory Action, the Examiner also stated that transistors 11 and 13 are substantially different from transistor 12 because transistors 11 and 13 have much larger gates than transistor 12. However, the Examiner has not pointed to, nor is applicant's attorney aware, of any teaching that indicates that the size of a MOS transistor gate is inherently related to the thickness of the gate oxide layer. In other words, applicant's attorney is unaware of any teaching that indicates that as the size of the gate increases, the thickness of the gate oxide must also increase.

In the Advisory Action, the Examiner further stated that Ariizuma shows that gate oxides 20 and 21 are thinner than gate oxide 19. Applicant notes, however,

that the claims do not recite that the first gate oxide is thinner than the second gate oxide, but instead require that the thickness of the first gate oxide be substantially less than the thickness of the second gate oxide. As noted above, the Ariizuma reference does not teach or suggest this limitation.

With further respect to claim 3 (previous claim 10), claim 3 requires that the third transistor be substantially non-conductive when zero volts are applied to the gate. As noted above, the Examiner pointed to transistor 11 shown in FIG. 4 of Ariizumi as constituting the first transistor of the claims, and transistor 12 shown in FIG. 4 of Ariizumi as constituting the second transistor of the claims. In addition, the Examiner appears to point to transistor 13 shown in FIG. 4 of Ariizumi as constituting the third transistor of the claims.

However, as shown in FIG. 4 of Ariizumi, transistor 13 is a depletion-mode device. As a result, it is not possible for transistor 13 to be substantially non-conductive when zero volts are applied to the gate because a depletion-mode device is conductive when zero volts are applied to the gate. From what applicant can determine, the Examiner did not address these comments in the Advisory Action.

With further respect to claim 6 (previous claim 13), claim 6 recites, in part,

> "wherein the first and third transistors have source and drain regions of the same conductivity type, and the second transistor has source and drain regions of an opposite conductivity type."

As noted above, the Examiner pointed to transistor 11 shown in FIG. 4 of Ariizumi as constituting the first transistor of the claims, and transistor 12 shown in FIG. 4 of Ariizumi as constituting the second transistor of the claims. In addition, the Examiner appeared to point to transistor 13 shown in FIG. 4 of Ariizumi as constituting the third transistor of the claims.

Applicant notes, however, that one skilled in the art would not be motivated to form transistor 13 shown in FIG. 4 of Ariizumi as a PMOS device because the invention of Ariizumi would no longer function as intended. Transistor 13 of FIG. 4

of Ariizumi is shown as a diode-connected NMOS transistor. As noted by Ariizumi, the gate of transistor 13 is protected from voltage spikes on the VCC terminal because the gate and drain of transistor 13 are connected together. (See column 3, lines 56-59 of Ariizumi.)

However, if a diode-connected PMOS transistor were used in lieu of NMOS transistor 13, the gate would no longer be protected. Thus, voltage spikes on the source of a PMOS transistor from the VCC terminal can destroy the gate. As a result, one skilled in the art would not be motivated to use a PMOS transistor in lieu of NMOS transistor 13. Thus, one skilled in the art would not be motivated to change transistor 13 (the third transistor) so that transistor 13 and transistor 12 (the second transistor) have opposite conductivity type. From what applicant can determine, the Examiner did not address these comments in the Advisory Action.

Respectfully submitted,

Dated: 10-22-03 By: _____

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